

WHAT IS CLAIMED IS:

1. A process for fabricating membrane-substrate structures comprising:
 - providing a substrate;
 - depositing a protective layer on said substrate;
 - forming a trench in said substrate, said trench having a trench depth;
 - depositing a first intermediate layer in said trench;
 - depositing a sacrificial layer on said first intermediate layer, said sacrificial layer having a sacrificial layer depth;
 - depositing and patterning a second intermediate layer on said sacrificial layer;
 - depositing a layer of polymeric material on said second intermediate layer and said sacrificial layer, said layer of polymeric material contacting said second intermediate layer;
 - removing said sacrificial layer; and
 - forming an air gap between the layer of polymeric material and the substrate by release of said layer of polymeric material upon removal of said sacrificial layer, whereby said air gap has an air gap depth greater than said sacrificial layer depth.
2. The process of claim 1, wherein said substrate comprises silicon.
3. The process of claim 2, wherein said protective layer is made of Si_xN_y or SiO_2 , wherein x and y are greater than zero, x being less than y.
4. The process of claim 1, wherein said substrate comprises GaAs.
5. The process of claim 4, wherein said protective layer is made of Si_xN_y , wherein x and y are greater than zero, x being less than y.
6. The process of claim 1 further comprising the steps of:

curing said layer of polymeric material;
depositing a mask on said layer of polymeric material;
patterning said mask to have mask holes;
etching said layer of polymeric material in correspondence of the mask holes, thus providing film holes in the layer of polymeric material; and
removing said mask before removing said sacrificial layer.

7. The process of claim 3, wherein said layer of Si_xN_y or SiO_2 is $0.5 \mu\text{m}$ thick.
8. The process of claim 3, wherein said layer of Si_xN_y is deposited onto said wafer by plasma enhanced chemical vapor deposition or low pressure chemical vapor deposition.
9. The process of claim 3, wherein said layer is made of SiO_2 and is deposited onto said substrate by thermal deposition.
10. The process of claim 5, wherein said layer is made of Si_xN_y and is deposited onto said substrate by plasma enhanced chemical vapor deposition or low pressure chemical vapor deposition.
11. The process of claim 1, wherein said trench is etched in said substrate using a KOH solution.
12. The process of claim 1, wherein said trench is etched in said substrate using ethylene diamine pyrocatechol.
13. The process of claim 1, wherein said trench has a depth of between about $5 \mu\text{m}$ and $50 \mu\text{m}$.
14. The process of claim 1, wherein said metal comprises a Ti-Au film having a thickness of about $1 \mu\text{m}$.

15. The process of Claim 1, wherein said membrane pad comprises a Ti-Au film having a thickness of about 1 μ m.
16. The process of claim 1, wherein said sacrificial layer comprises metal, PECVD SiO₂, or KCl.
17. The process of claim 1, wherein said polymeric material is polyimide.
18. The process of claim 6, wherein said polymeric material is polyimide and is cured at a temperature of about 300 °C.
19. The process of claim 18, wherein said polyimide shrinks by about 20-40% upon curing.
20. The process of claim 6, wherein said mask comprises a mask metal.
21. The process of claim 20, wherein said mask metal is Al.
22. The process of claim 6, wherein said polymeric material is etched by reactive ion etching.
23. The process of claim 6, wherein said mask is removed by an etchant and said sacrificial layer is removed by BOE or hot deionized water.
24. The process of claim 1, wherein said sacrificial layer comprises at least one of KCl and PECVD SiO₂.
25. The process of claim 1, further comprising:
removing the protective layer.
26. A process for fabricating membrane-substrate structures comprising the steps of:

providing a substrate having a one side and an other side;
depositing a first protective layer on said one side and a second protective layer on said other side;
forming a trench in said substrate, said trench having a trench depth;
depositing a third protective layer in said trench;
depositing a first intermediate layer on said third protective layer;
depositing a sacrificial layer on said first intermediate layer and said third protective layer, said sacrificial layer having a sacrificial layer depth;
depositing a second intermediate layer on said sacrificial layer;
depositing a layer of polymeric material on said first protective layer, said second intermediate layer, and said sacrificial layer;
removing said sacrificial layer; and
forming an air gap between the layer of polymeric material and the substrate by release of said layer of polymeric material from said sacrificial layer upon removal of said sacrificial layer, whereby said air gap has an air gap depth greater than said sacrificial layer depth.

27. The process of claim 26, wherein said substrate comprises silicon.
28. The process of claim 27, wherein said first protective layer, said second protective layer, and said third protective layer comprise Si_xN_y or SiO_2 , x and y being greater than zero, x being less than y.
29. The process of claim 26, wherein said substrate comprises GaAs.
30. The process of claim 29, wherein said first protective layer, said second protective layer, and said third protective layer comprise Si_xN_y , x and y being greater than zero, x being less than y.
31. The process of claim 26, wherein said step of removing said sacrificial layer comprises the steps of:
providing access holes in said second protective layer;

etching a portion of the substrate above said access holes; and removing said third protective layer and said sacrificial layer.

32. The process of claim 28, wherein said layer of Si_xN_y or SiO_2 is 0.5 μm thick.
33. The process of claim 28, wherein said first protective layer, second protective layer, and third protective layer comprise Si_xN_y and are deposited onto said substrate by plasma enhanced chemical vapor deposition or low pressure chemical vapor deposition.
34. The process of claim 28, wherein said first protective layer, second protective layer, and third protective layer comprise SiO_2 and are deposited onto said wafer by thermal deposition.
35. The process of claim 30, wherein said first protective layer, second protective layer, and third protective layer are deposited onto said wafer by plasma enhanced chemical vapor deposition or low pressure chemical vapor deposition.
36. The process of claim 26, wherein said trench is etched in said substrate using a KOH solution.
37. The process of claim 26, wherein said trench is etched in said substrate using ethylene diamine pyrocatechol.
38. The process of claim 26, wherein said trench has a depth of between about 5 μm and about 50 μm .
39. The process of claim 26, wherein said metal comprises a Ti-Au film having a thickness of about 1 μm .
40. The process of Claim 26, wherein said second intermediate layer comprises a Ti-Au film having a thickness of about 1 μm .

41. The process of claim 26, wherein said sacrificial layer comprises metal, PECVD SiO₂, or KCl.
42. The process of claim 26, wherein said polymeric material is polyimide.
43. The process of claim 26, wherein said polymeric material is cured at a temperature of about 300°C.
44. The process of claim 43, wherein said polymeric material shrinks by about 20-40% upon curing.
45. The process of claim 31, wherein said polymeric material is etched by reactive ion etching.
46. The process of claim 31, wherein said sacrificial layer is removed by BOE or hot deionized water.
47. The process of claim 26, wherein said sacrificial layer comprises at least one of KCl and SiO₂.
48. The process of claim 26, further comprising the step of:
removing the first protective layer.
49. A process for restoring tensile stress to a monolithic membrane-substrate structure comprising the steps of:
a) fabricating a membrane-substrate structure, said step of fabricating the membrane-substrate structure comprising:
 - a1) providing a substrate having a one side and an other side;
 - a2) depositing a first protective layer on said one side and a second protective layer on said other side;

- a3) forming a trench in said substrate, said trench having a trench depth;
- a4) depositing a third protective layer in said trench;
- a5) depositing a first intermediate layer on said third protective layer;
- a6) depositing a sacrificial layer on said first intermediate layer and said third protective layer, said sacrificial layer having a sacrificial layer depth;
- a7) depositing a second intermediate layer on said sacrificial layer;
- a8) depositing a layer of polymeric material on said first protective layer, said second intermediate layer, and said sacrificial layer;
- a9) removing said sacrificial layer; and
- a10) forming an air gap between the layer of polymeric material and the substrate by release of said layer of polymeric material from said sacrificial layer upon removal of said sacrificial layer, whereby said air gap has an air gap depth greater than said sacrificial layer depth;

- b) providing a wafer;
- c) disposing said membrane-substrate structure on said wafer;
- d) heating said wafer and said membrane-substrate structure; and
- e) cooling said wafer and said membrane-substrate structure to room temperature.

50. The method of claim 49, wherein said wafer and said membrane-substrate structure are heated to about 300°C.

51. A process for restoring tensile stress to a monolithic membrane-substrate structure comprising the steps of:

- a) fabricating a membrane-substrate structure, said step of fabricating the membrane-substrate structure comprising:
 - a1) providing a substrate;
 - a2) depositing a protective layer on said substrate;
 - a3) forming a trench in said substrate, said trench having a trench depth;
 - a4) depositing a first intermediate layer in said trench;
 - a5) depositing a sacrificial layer on said first intermediate layer, said sacrificial layer having a sacrificial layer depth;

- a6) depositing and patterning a second intermediate layer on said sacrificial layer;
- a7) depositing a layer of polymeric material on said second intermediate layer and said sacrificial layer, said layer of polymeric material contacting said second intermediate layer;
- a8) removing said sacrificial layer; and
- a9) forming an air gap between the layer of polymeric material and the substrate by release of said layer of polymeric material upon removal of said sacrificial layer, whereby said air gap has an air gap depth greater than said sacrificial layer depth;

- b) providing a wafer;
- c) disposing said membrane-substrate structure on said wafer;
- d) heating said wafer and said membrane-substrate structure; and
- e) cooling said wafer and said membrane-substrate structure to room temperature.

52. The method of claim 51, wherein said wafer and said membrane-substrate structure are heated at about 300 °C.

53. A monolithic membrane-substrate structure, comprising:

- a substrate having a trench, said trench having a trench depth;
- a protective layer located on the substrate;
- a layer of polymeric material located above the substrate and the protective layer;
- a first intermediate layer located in said trench;
- a second intermediate layer located under said layer of polymeric material and contacting said layer of polymeric material; and
- an air gap between the layer of polymeric material and the substrate.

54. A monolithic membrane-substrate structure, comprising:

- a substrate having a first side;
- a first protective layer disposed on the first side of the substrate;

a second protective layer disposed on the second side of the substrate;
a third protective layer disposed on the first side of the substrate;
a layer of polymeric material located above the first and third protective layer;
a first intermediate layer located above said third protective layer and contacting said third protective layer;
a second intermediate layer located under said layer of polymeric material and contacting said layer of polymeric material; and
an air gap between the layer of polymeric material and the substrate.